W-CDMA 1chip SiGe TX-IC with high dynamic range and accurate temperature compensation VGA

Hideyuki Nakamizo, Tetsuya Ueda, Keiji Ninomiya, Yoshinori Takahashi, Yoshinori Matsunami, Hiroyuki Joba, Kenji Itoh, †Duljit S. Malhi, †Dawn Wang

Mobile Terminal Center, Mitsubishi Electric Corporation
8-1-1, Tsukaguchi-honmachi, Amagasaki, Hyogo 661-8661, Japan
†Boston Design Center, TriQuint Semiconductor, Lowell, MA

Abstract — **This paper demonstrates the 1chip SiGe TX-IC for W-CDMA mobile terminals. For the TX-IC, a novel architecture of a variable gain amplifier is proposed to improve temperature compensation of gain and distortion. And current consumption of variable gain amplifier can be reduced with power control level and it is constant over temperature. The current consumption of the TX-IC is 84 mA with output power of +7 dBm, and it is reduced to 63 mA with output power of -83.5 dBm. With the 0.25 μm SiGe BiCMOS technology, this TX-IC achieved high dynamic range over 100dB within ±2.5 dB accuracy over temperature.**

I. Introduction

The popularization of the cellular phone brought higher demand of the small size, highly efficient terminal in the market.. The W-CDMA service was launched in Japan by NTT DoCoMo in 2002. The W-CDMA system is expected its high transmission rate for multimedia usage. The market requires a larger display and applications with higher layer. For the small size terminal, miniaturization and low current consumption of each component are always necessary. For the TX-IC consisted of transmitter functionalities except a HPA, low current consumptions and small sized implementation are needed. Also the W-CDMA system requires high dynamic range, high accuracy for power control and low distortion. These requirements of the W-CDMA system are defined in 3GPP [1]. For such requirements in W-CDMA TX-ICs, BiCMOS IF-IC [2] GaAs RF-IC [3] and SiGe TX-IC [4] are presented.

In this paper, the W-CDMA 1chip SiGe TX-IC is described. This TX-IC is implemented with the use of SiGe BiCMOS for the fully integration of TX blocks with synthesizer blocks. The TX blocks consist of the balanced I/Q modulator (I/Q-MOD), the IF variable gain amplifier (IF-VGA), the Up-converter (UP-MIX), the RF variable gain amplifier (RF-VGA) and the driver amplifier (RF-AMP). This TX-IC has the IF and the RF synthesizer blocks with the serial interface. Both of the synthesizer blocks consist of the voltage controlled oscillator (VCO) and the phase locked loop (PLL).

The novel architecture of the IF-VGA is proposed to improve temperature compensation of gain and distortion. And current consumption of variable gain amplifier can be reduced with power control level and it is constant over temperature. In following discussions on the IF-VGA circuit schematic and its behavior are described.

II. Architecture and Circuit Design

A. Architecture

In general, the W-CDMA transmitter consists of an antenna, a RF switch, a duplexer, an isolator, a HPA, a RF SAW and a TX-IC. Base-band differential input signals (I,Q) are provided from the base-band IC. Reference frequency for the PLL is provided from the TCXO. The TX-IC is required the power control range of 95 dB as a minimum requirement [4].

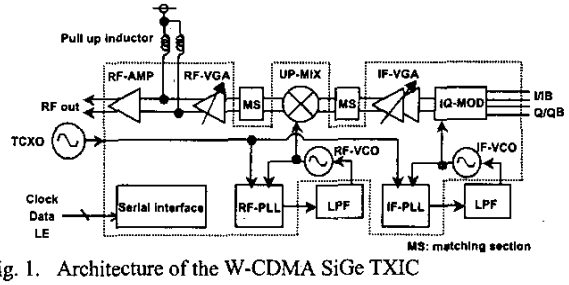

Fig. 1. Architecture of the W-CDMA SiGe TXIC

Fig.1 shows the block diagram of the highly integrated dual up-conversion W-CDMA transmitter. The TX blocks and the synthesizer blocks are connected internally on the silicon. And the I/Q-MOD and the IF-VGA are connected internally on the silicon. The pull up inductors of the RF-VGA are off-chip.

In this paper, details of the TX blocks are described as follows.

0-7803-7694-3/03/$17.00 © 2003 IEEE

B. I-Q Modulator (I/Q-MOD)

The I/Q-MOD employs the double balanced BiCMOS Gilbert cell mixer architecture. The base band I/Q inputs are fed into NFET differential pairs of the Gilbert cell. LO differential input signal is supplied from the IF synthesizer block connected internally.

C. IF Variable Gain Amplifier (IF-VGA)

The block diagram of the IF-VGA is shown in Fig.2. The IF-VGA includes two stage cascaded VGAs. The first stage VGA (VGA-1) is the circuit of which gain is in proportion to temperature and input dynamic range does not depend on temperature. This contributes to temperature compensation of gain and distortion of the IF-VGA. The second stage VGA (VGA-2) is the current-controlled type VGA. This contributes to linear gain control range more than 80 dB and current reduction at low gain setting.

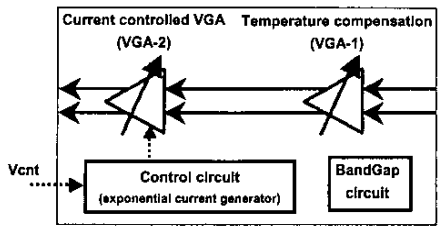

Fig. 2. The block diagram of the IF-VGA

This IF-VGA has technical features as follows:

(a) The current-controlled VGA with linear gain control.
(b) Temperature compensation for gain and distortion.
(c) Constant current consumption over temperature.

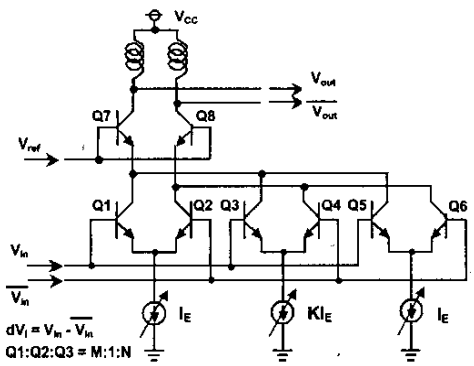

Fig. 3. The circuit schematic of the VGA-2 core

Firstly, the technical feature (a) is discussed. Fig.3 shows the core circuit schematics of the VGA-2. It is multi-tanh triplet structure [5] in order to ensure larger input dynamic range than a single differential pair. Transistor ratio M, N and current ratio K are optimized. Cascade transistor (Q7, Q8) contributes better isolation between signal input and output. Dynamic range greater than 80dB is achieved by varying I_E, the emitter bias current, and current consumption of the VGA-2 at low gain can be reduced. Since gain is in proportion to log of I_E, gain control with high linearity is achieved by applying exponential current generator to gain control circuit. Fig.4 shows the gain control characteristic of the VGA-2.

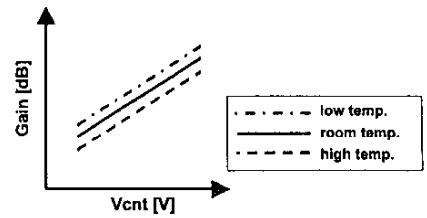

Fig. 4. The gain control characteristic of the VGA-2

Secondly, the technical feature (b) is discussed. Gain of the VGA-2 is controlled by varying I_E .In this architecture, the functional form of its dc transfer function is shown as following.

$$dI = I_E\left(\tanh\left(\frac{dV_i}{2V_T}+A\right)+K\tanh\left(\frac{dV_i}{2V_T}\right)+\tanh\left(\frac{dV_i}{2V_T}-A\right)\right) \quad (1)$$

where

$$A=\frac{\ln(M)}{2} \quad (2)$$

dI is the differential output current, dV_i is the differential input voltage and V_T has usual meaning of kT/q. And it follows that gain and third harmonics distortion (HD3) [5] are function of dV_i/V_T as following.

$$\text{Gain}=\frac{I_E}{2}(2+K-2\tanh^2(A))\times\left(\frac{dV_i}{V_T}\right) \quad (3)$$

$$HD3=-\left(\frac{2+K-8\tanh^2(A)+6\tanh^4(A)}{48(2+K-2\tanh^2(A))}\right)\times\left(\frac{dV_i}{V_T}\right)^2 \quad (4)$$

Gain and HD3 have temperature characteristics as above expressions at the condition of small input signal. Gain drops at high temperature and HD3 degrades at low temperature. Concerning the VGA-1, differential output voltage amplitude is in proportion to temperature and input dynamic range does not depend on temperature. It follows that temperature characteristics of the VGA-1 gain and the VGA-2 gain are cancelled. Also, the VGA-2 obtains input signal having gain characteristic in proportion to temperature from the VGA-1. It follows that temperature

characteristic of HD3 of the IF-VGA becomes constant over temperature.

Lastly, the technical feature (c) is discussed. To compensate the gain of the VGA-2 over temperature, current consumption has to be in proportion to temperature. In this IF-VGA, since output power of the VGA-1 is in proportion to temperature, temperature characteristics of the VGA-2 gain can be supplemented and it follows that the excess current at high temperature can be saved and current consumption becomes constant over temperature. There is advantage to current consumption of the IF-VGA with this structure in the case that current consumption of the VGA-1 is smaller than the excess current. In this IF-VGA, since current consumption of the VGA-1 is 2.4 mA and the excess current of the VGA-2 is 3.5 mA, current of 1.1 mA can be reduced at high temperature.

This IF-VGA offers the gain control range over 80 dB with high linearity and output P1dB of +1.4 dBm. The temperature variation of output P1dB is only 0.5dB. Current consumption is 11 mA with output of -14 dBm and it can be reduced to 6.3 mA with output of -93 dBm.

D. RF Up-Converter (UP-MIX)

The UP-MIX is a balanced Gilbert style mixer with a resistive feedback between Collector and Base in the lower differential pair to achieve the desired gain and IP3. The upper quad HBT's behave as switch. LO differential input signal is supplied from RF synthesizer block connected internally.

E. RF Variable Gain Amplifier (RF-VGA)

The RFVGA employs the multi-tanh triplet architecture same as the second stage of the IFVGA. The difference between the second stage of IF-VGA and RF-VGA is the temperature characteristic of I_E. In this RF-VGA, temperature compensation of gain is implemented by supplying current in proportion to temperature from gain control circuit. This RF-VGA offers the gain control range over 40 dB with high linearity and the highest gain of 15 dB. It consumes 19 mA while providing +3 dBm of OP1dB. Current consumption of the RF-VGA can be reduced to 1.1 mA at –25 dB gain. DC cut capacitors between the RF-VGA and the RF-AMP are integrated on the silicon to reduce the off-chip components and the pull up inductors of the RF-VGA allow off-chip matching flexibility to improve linearity and gain for differential operation. BandGap circuit is shared with the RF-AMP.

F. Driver Amplifier (RF-AMP)

The RF-AMP is a single-stage common emitter amplifier with a resistive feedback between Collector and Base for improved stability and linearity. Since this RFAMP is a differential amplifier, the influence of parasitic inductance of ground bonding wire can be ignored. This RF-AMP offers 14 dB gain and +13.5 dBm of OP1dB while consuming only 14 mA of quiescent current.

G. Synthesizer block

Synthesizer block (IF-VCO, IF-PLL, RF-VCO, RF-PLL and Serial interface) is fully integrated on the TX-IC without the loop filter components. This integration contributes a reduction of RF portion on PCB board of mobile terminal. And current consumption of the LO buffer can be reduced by employing internal connection between VCO and Mixer circuit.

III. Experimental Results

The TX-IC for W-CDMA mobile terminals was implemented using 0.25 μm SiGe BiCMOS production technology. A photomicrograph of the chip is shown in Fig. 5. The active area of the IC is 3.74 mm × 3.74 mm and is compatible to be packaged in a 40 pin, QFN40.

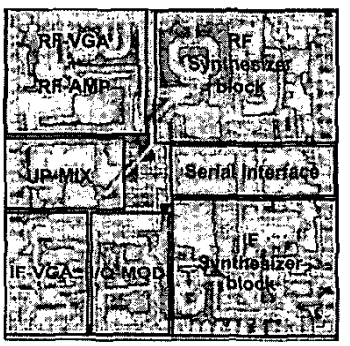

Fig. 5. Photomicrograph of the TX-IC chip

The Power Control Characteristic of the IF-VGA over temperatures is shown in Fig. 6. Power control from -93 dBm to -4 dBm is confirmed by this measurement results. Another feature characteristic of the IF-VGA is temperature characteristic. The gain error variation from room temperature is shown in Fig. 7. It is confirmed that Gain control curve slides parallel to the curve of room temperature within ±1.5 dB over the power range from -90 dBm to -4 dBm by this measurement results. Current consumption of the IF-VGA is also shown in Fig. 8. It is confirmed that current consumption of the IF-VGA is constant over temperature and it can be reduced at low output power.

For the RF-VGA, the gain control range from -25 dB to 15 dB with high linearity is confirmed by the measurement results. It is also confirmed the gain error variation from room temperature is ±1.0 dB.

Measurements on individual building blocks and fully cascaded TX chains with synthesizer are performed, and results are shown in Table I. The total current consumption of the TX-IC is approximately 84 mA when the power of the RF-AMP output is +7 dBm. Since current consumption varies with power control level, it is reduced to 63 mA at output of -83.5dBm.

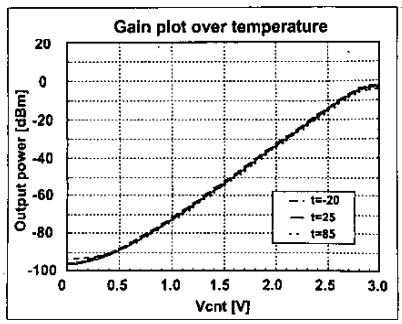

Fig. 6. The power control characteristic of the IF-VGA

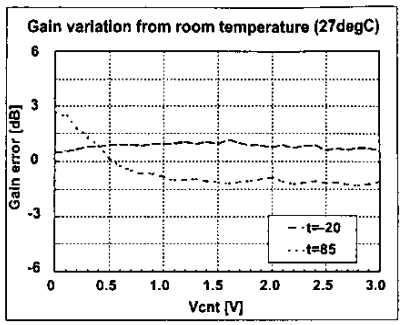

Fig. 7. The gain variation characteristic of the IF-VGA

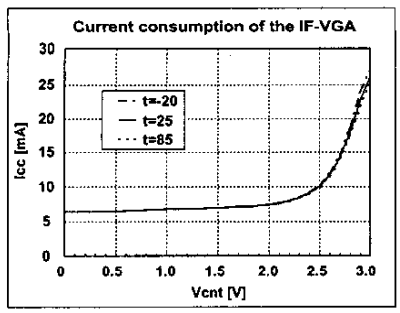

Fig. 8. Current consumption of the IF-VGA

IV. Conclusion

SiGe 1chip TX-IC for W-CDMA mobile terminals with the novel architecture of a variable gain amplifier is proposed to improve temperature compensation of gain and distortion. With 0.25 μm SiGe BiCMOS technology, this TX-IC achieved dynamic range over 100 dB (IF-VGA: 80 dB, RF-VGA: 40dB) within ±2.5 dB accuracy over temperature. The maximum output modulated power of +7 dBm, -45 dBc ACLR at 5 MHz offset is achieved. Measurement results also satisfy the specification defined by 3GPP. It consumes 250 mW of +7 dBm output power for typical voltage supply of 3.0 V, and it varies with power control level.

TABLE I
MEASUREMENT RESULTS OF TX-IC

Maximum CH Power	7.0 dBm	@1950 MHz
Minimum CH Power	-83.5 dBm	@1950 MHz
Power Control Range	90.5 dB	@1950 MHz
OBW	4.3 MHz	@+7 dBm output
ACLR	-46.8 dBc	@+5 MHz
	-45.6 dBc	@-5 MHz
	-66.3 dBc	@+10 MHz
	-62.4 dBc	@-10 MHz
Current consumption	84 mA	@+7 dBm output
	63 mA	@-83.5 dBm output

Acknowledgments

The authors would like to acknowledge TriQuint Semiconductor's design team for the co-development on the TX-IC.

References

[1] 3GPP TS34.121, 3rd generation partnership project; technical specification group terminal; terminal conformance specification; radio transmission and reception (FDD), Release 1999.

[2] S. Otaka, G. Takemaru etc. "A Low –Power Low Noise Accurate Linear-in-dB Variable-gain Amplifier with 500-MHz Bandwidth", IEEE Journal of Solid-State Circuits, Vol. 35, NO. 12, December 2000.

[3] W. Thomann, J. Fenk, R. Hagelauer, "Fully Integrated W-CDMA IF Receiver and IF transmitter Including IF Synthesizer and On-Chip VCO for UMTS Mobiles", IEEE Journal of Solid-State Circuits, Vol. 36, NO. 9, September 2001.

[4] H. Joba, Y. Takahashi, Y. Matsunami etc. "W-CDMA SiGe TX-IC with high dynamic range and high power control accuracy ", 2002 IEEE Radio Frequency integrated Circuits (RFIC) Symposium, Seattle, WA –June 2-4, 2002, pp. 27-30.

[5] B. Gilbert, "The Multi-tanh Principle:A tutorial Overview", IEEE Journal of Solid-State Circuits, Vol. 33, NO. 1, January 1998.